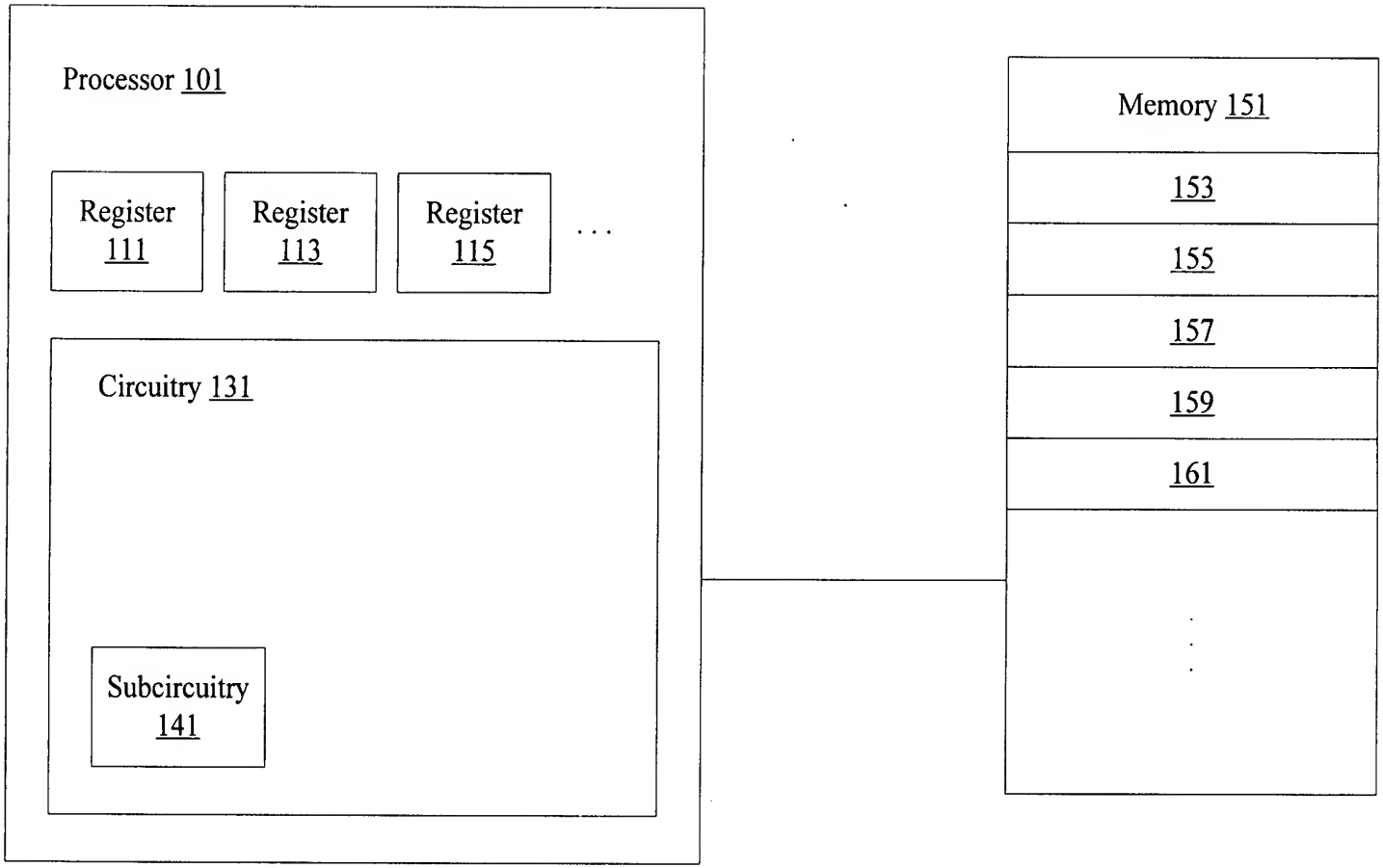

Processor 101
Register 111
Register 113
Register 115
. . .
Circuitry 131
Subcircuitry 141
Memory 151
153
155
157
159
161

Figure 1

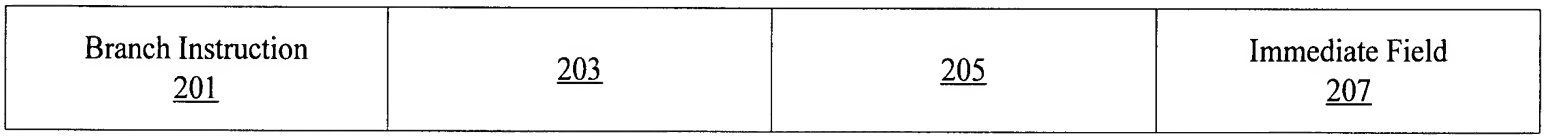


Figure 2

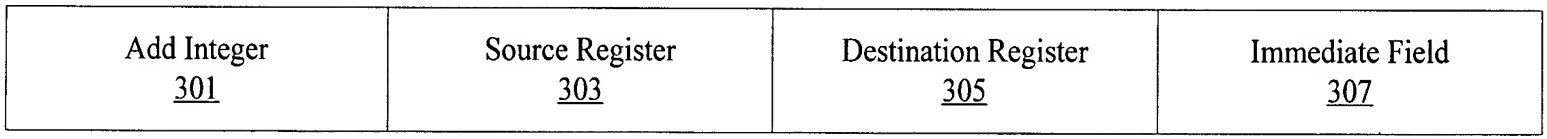

Add Integer
301
Source Register
303
Destination Register
305
Immediate Field
307

Figure 3

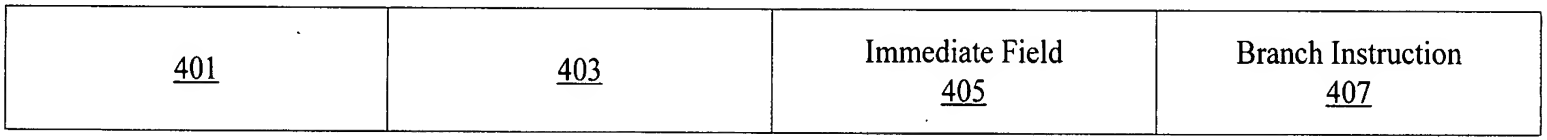


Figure 4

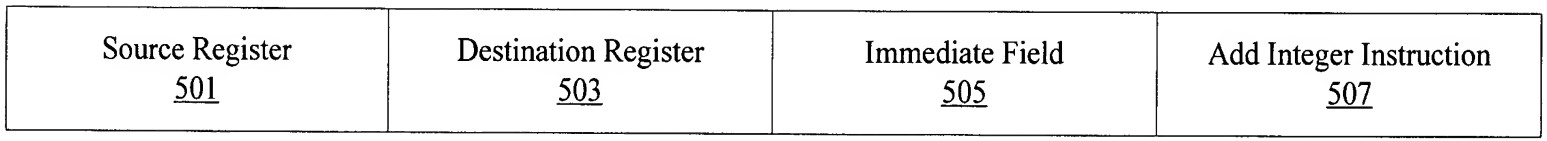

Source Register
501
Destination Register
503
Immediate Field
505
Add Integer Instruction
507

Figure 5

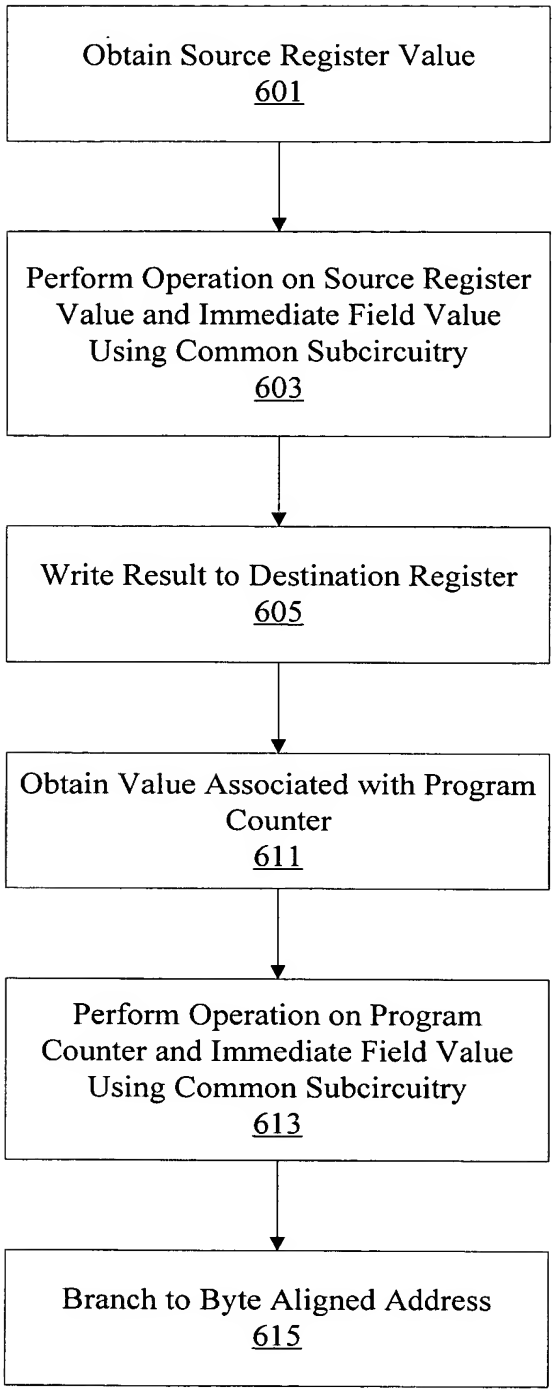

Obtain Source Register Value
601
Perform Operation on Source Register Value and Immediate Field Value Using Common Subcircuitry
603
Write Result to Destination Register
605
Obtain Value Associated with Program Counter
611
Perform Operation on Program Counter and Immediate Field Value Using Common Subcircuitry
613
Branch to Byte Aligned Address
615

Figure 6

Figure 7

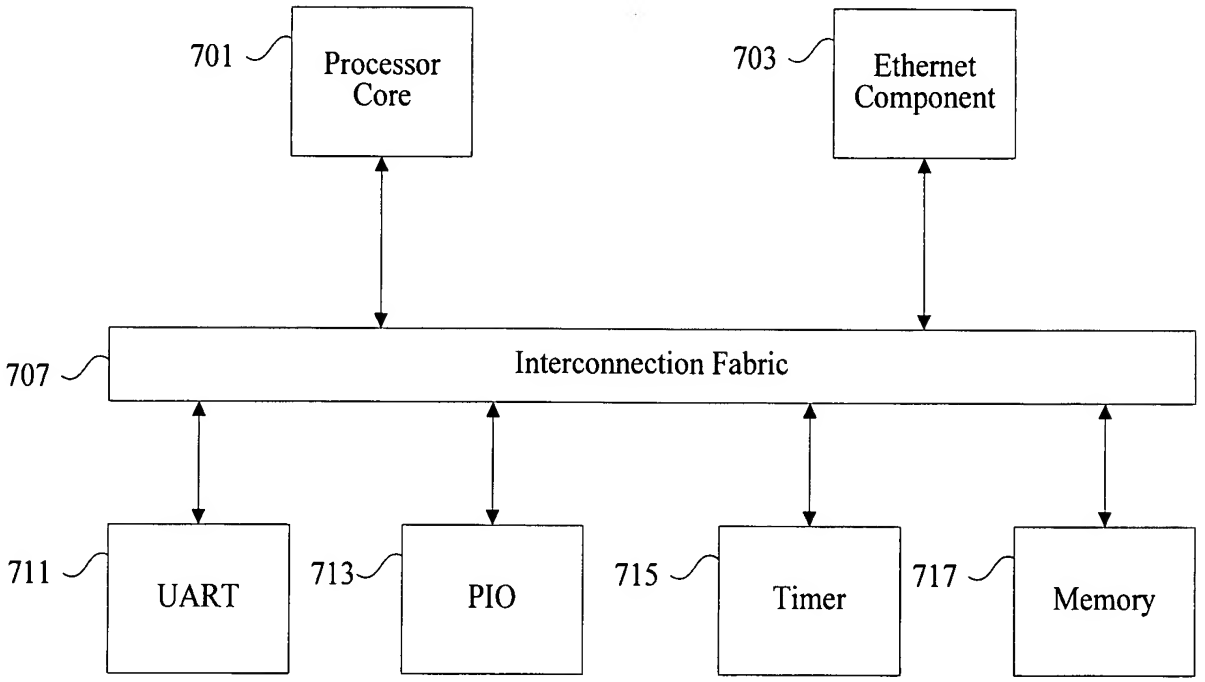
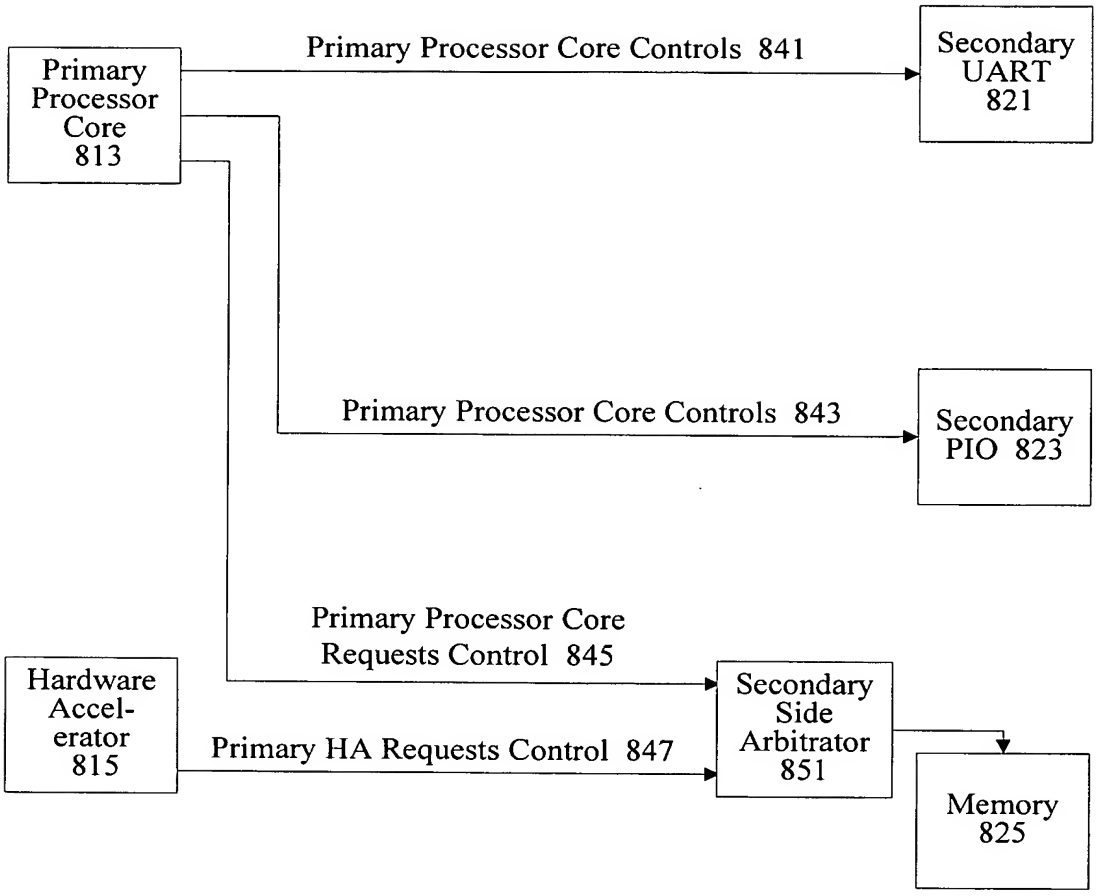

701
Processor Core
703
Ethernet Component
707
Interconnection Fabric
711
UART
713
PIO
715
Timer
717
Memory

Figure 8


Primary Processor Core 813
Primary Processor Core Controls 841
Secondary UART 821
Primary Processor Core Controls 843
Secondary PIO 823
Primary Processor Core Requests Control 845
Hardware Accel-erator 815
Primary HA Requests Control 847
Secondary Side Arbitrator 851
Memory 825

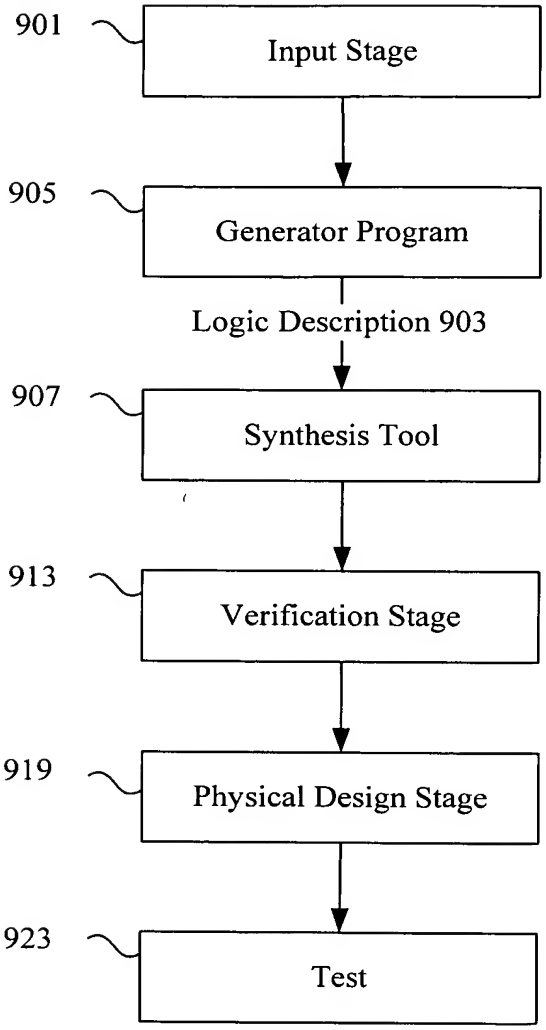

901
Input Stage
905
Generator Program
Logic Description 903
907
Synthesis Tool
913
Verification Stage
919
Physical Design Stage
923
Test

Figure 9

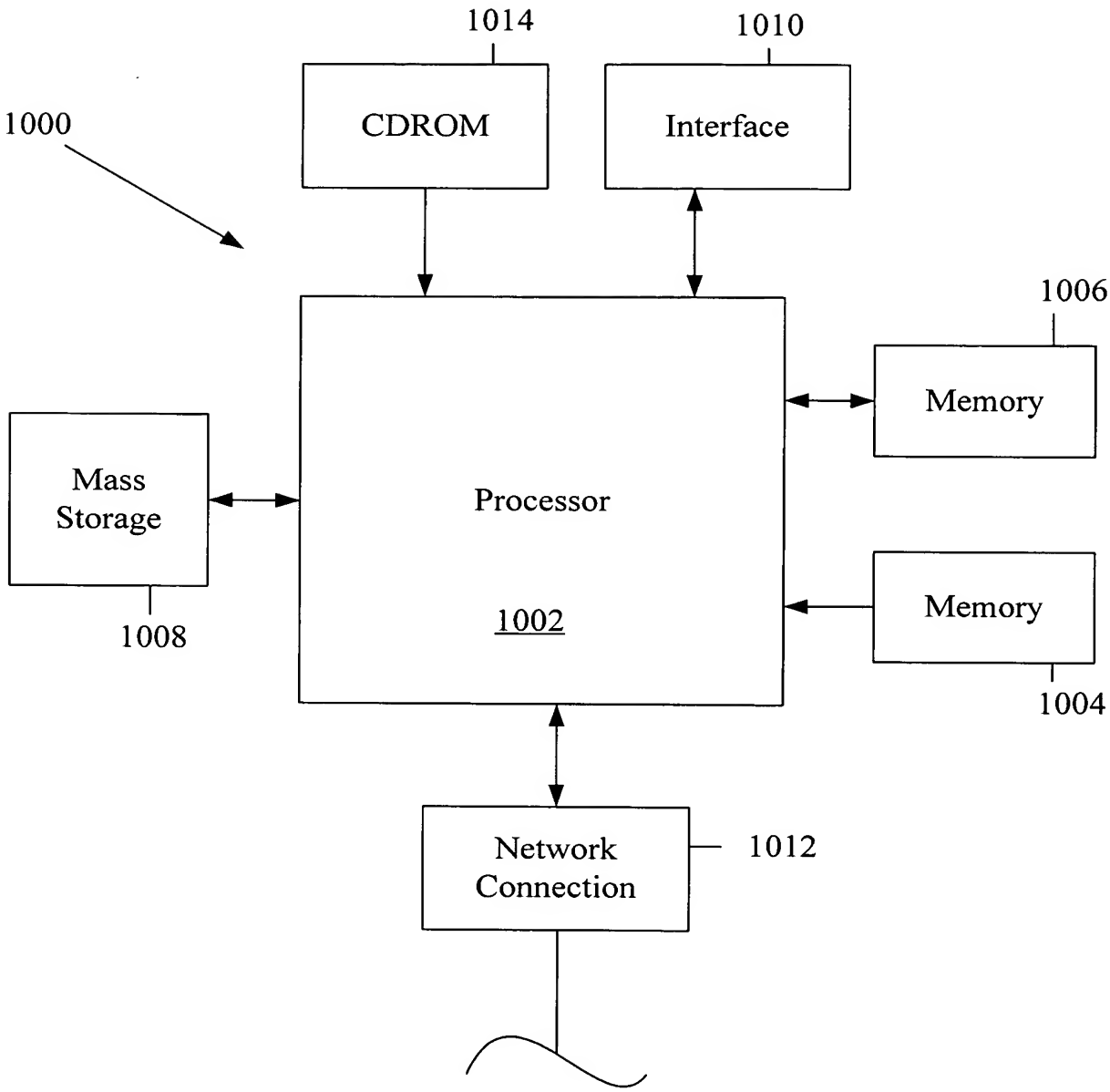

1014
1010
1000
CDROM
Interface
1006
Memory
Mass
Storage
Processor
1002
Memory
1008
1004
Network
Connection
1012

Figure 10